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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:	)	Group Art Unit: 2811
TAKEUCHI	)	
Serial No. 09/930,365	)	Examiner: Vu
Filed: June 19, 2001	)	
For: METHODS FOR MANUFACTURING SEMICONDUCTOR DEVICES AND SEMICONDUCTOR DEVICES HAVING TRENCH ISOLATION REGIONS	)	

AMENDMENT

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

In response to the Office Action dated June 18, 2002, the response being due by December 18, 2002 by the enclosed petition for extension of time, please enter and consider the following.

IN THE CLAIMS:

Please cancel claims 6 and 27-31 without prejudice.

Please amend claims 1, 7, 14 and 19 as follows:

1. (amended) A method for manufacturing a semiconductor device having a trench isolation region, the method comprising the steps of:

(a) forming a trench in a semiconductor layer;

(b) forming a dielectric layer that fills the trench;

(c) conducting a thermal treatment of the dielectric layer, wherein the thermal treatment is conducted at temperatures of at least 1050°C; and

(d) forming a well in the semiconductor layer, and the step (c) is conducted before the step (d).